heat slug is attached to the substrate by an adhesive. The method includes: preparing a semiconductor chip having conductive bumps on the front surface of the semiconductor chip; bonding a heat slug on the backside of the semiconductor chip using a solder film; and attaching the semiconductor chip on the substrate such that the conductive bumps of the semiconductor chip contact bonding pads of the substrate.

cont. All

REMARKS

The above amendment amends the specification to correct obvious errors and improve grammar. No new matter is added.

The drawings were objected to as failing to comply with 37 C.F.R. § 1.84(p)(4) because reference character "14" has been used to designate both adhesion layer and the metal layer. Page 4, lines 8 and 21-23 (before amended) reads, "an adhesion layer is formed" and "[t]he layer 14, which promotes the adhesion between the semiconductor chip 10 and the solder film 30, typically has a multi-layer metal structure." Because adhesion layer 14 is made of a multi-layer metal, "the metal layer" was used with reference character "14". However, in order to improve the clarity of the specification, the specification is amended to show that the reference character "14" designate adhesion layer. Accordingly, Applicants request withdrawal of the objection under 37 C.F.R. § 1.84(p)(4).

The drawings were objected to because it is not clear to the Examiner which part of Fig. 1 is being enlarged. The part of the specification that describes the drawings is amended to make the description of the drawings clear. Accordingly, Applicants request withdrawal of the objection.

The disclosure was objected to because of a number of informalities. The disclosure is amended to remove the informalities. Figs. 1 and 3 are amended to remove reference numbers 42, 61, and 62. Amendment of the drawings is shown in red ink on the attached sheets, which is accompanied by a request to amend the drawings under 37 C.F.R. § 1.121. Formal drawings incorporating the changes will be submitted after the Examiner's approval of the requested changes and an indication of allowable subject matter. Accordingly, Applicants request withdrawal of the objection.

The specification was objected to as failing to provide proper antecedent basis for "the metal layer 14" on page 6, line 5. As described above, "the metal layer 14" is amended to

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"the adhesion layer 14", which has proper antecedent basis on an adhesion layer 14 of page 4, lines 8. Accordingly, Applicants request withdrawal of the objection.

Claims 1, 11, and 14 were objected to because of a number of informalities. The claims are amended to remove the informalities. Accordingly, Applicants request withdrawal of the objection.

Claims 1-20 were pending in the above-identified application when last examined and are amended as indicated in Attachment B. Claims 1, 3, 6, 10, 11, 14, 15, and 20 are amended. The claim amendments clarify the claim language and are not intended to limit the scope of the claims, unless the claim language is expressly quoted in the following remarks to distinguish over the art cited.

Claims 3 and 15 were rejected under 35 U.S.C. § 112, second paragraph. Claim 3 is amended to clear the antecedent basis problem that the Examiner indicated, and claim 15 is amended to define the material filling the space. Applicants respectfully submit that claim 3 and 15 comply with the requirements of 35 U.S.C. § 112, second paragraph.

For the above reasons, Applicants request reconsideration and withdrawal of the rejection under 35 U.S.C. § 112.

Claims 1, 3, 6, 8, 9, 11, 14-17, and 19 were rejected under 35 U.S.C. § 102(b) as anticipated by U.S. patent No. 4,926,242 (Itoh). Applicants respectfully traverse the rejection.

Independent claim 1 distinguishes over Itoh at least by reciting, "a heat slug bonded to a backside of the semiconductor chip; and a solder film that bonds the heat slug to the backside of the semiconductor chip."

Itoh describes "a heat radiation structure that is excellent in heat conductivity." See col. 2, lines 26-27. Fig. 5 and col. 6, lines 55-66 of Itoh shows that semiconductor chip 54 is attached to envelope 52_1 through Mo plate 55 and solder layer 56 and that heat sink 51 is attached to envelope 52_1. Itoh discloses a heat sink attached not to a semiconductor chip, but to another structure (an envelope). Accordingly, since Itoh fails to teach or suggest "a heat slug bonded to a backside of the semiconductor chip; and a solder film that bonds the heat slug to the backside of the semiconductor chip", claim 1 is patentable over Itoh.

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Claims 3, 6, 8, 9, and 11 are patentable over Itoh for at least the reason of dependency on claim 1,which is patantable over Itoh.

Independent claim 14 distinguishes over Itoh at least by reciting, "bonding a heat slug on a backside of the semiconductor chip using a solder film."

Claim 14 is patentable over Itoh at least on the same ground that claim 1 is patentable over Itoh. Claim 15 is patentable over Itoh for at least the reason of dependency on claim 14.

Independent claim 16 distinguishes over Itoh at least by reciting, "a heat slug bonded to the semiconductor chip ... ; and a solder film that bonds the heat slug to the backside of the semiconductor chip."

Claim 16 is patentable over Itoh at least on the same ground that claim 1 is patentable over Itoh. Claims 17 and 19 are patentable over Itoh for at least the reason of dependency on claim 16.

For the above reasons, Applicants request reconsideration and withdrawal of the rejection under 35 U.S.C. § 102.

Claims 2 and 13 were rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. patent No. 4,926,242 (Itoh) in view of U.S. patent No. 5,359,768 (Haley). Applicants respectfully traverse the rejection.

Claim 4 was rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. patent No. 4,926,242 (Itoh) in view of U.S. patent No. 5,683,937 (Furukawa). Applicants respectfully traverse the rejection.

Claim 5 was rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. patent No. 4,926,242 (Itoh) in view of U.S. patent No. 5,811,317 (Maheshwari). Applicants respectfully traverse the rejection.

Claims 7 and 18 were rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. patent No. 4,926,242 (Itoh) in view of U.S. patent No. 5,336,364 (Takahama). Applicants respectfully traverse the rejection.

Claims 10 and 20 were rejected under 35 U.S.C. § 103(a) as unpatentable over U.S.

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patent No. 4,926,242 (Itoh) in view of U.S. patent No. 6,060,778 (Jeong). Applicants respectfully traverse the rejection.

Claim 12 was rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. patent No. 4,926,242 (Itoh). Applicants respectfully traverse the rejection.

As discussed above Itoh fails to teach or suggest the features recited in independent claims 1, 14, and 16. Haley, Furukawa, Maheshwari, Takahama, and Jeong also fail to teach or suggest the features recited in claims 1, 14, and 16. Accordingly, claims 1, 14, and 16 are patentable over Itoh, Haley, Furukawa, Maheshwari, Takahama, and Jeong, and claims 2, 4, 5, 7, 10, 12, 13, 18, and 20 are patentable over Itoh, Haley, Furukawa, Maheshwari, Takahama, and Jeong, respectively, for at least the reason of dependency on claims 1, 14, and 16, which are patentable.

In rejecting claims 10 and 20, the Examiner indicated that Jeong disclosed the anodizing layer recited in claims 10 and 20. Fig. 6 and col. 8, lines 3-5 of Jeong discloses anodizing layer 73a on the surface of second thermal conductive layer 73, on which integrated circuit chip 40 is bonded. Accordingly, Jeong fails to teach or suggest the anodizing layer recited in claims 10 and 20, which is "an anodizing layer on a surface of the heat slug that is opposite to another surface of the heat slug, on which the semiconductor chip is bonded."

For the above reasons, Applicants request reconsideration and withdrawal of the rejection under 35 U.S.C. § 103.

In summary, claims 1-20 were pending in the application. This response amends claims 1, 3, 6, 10, 11, 14, 15, and 20. For the above reasons, Applicants respectfully request allowance of claims 1-20. Should the Examiner have any questions concerning this response, the Examiner is invited to call the undersigned at (408) 453-9200.

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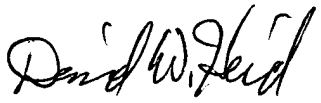
Respectfully submitted,



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ATTACHMENT A

In the following, insertions are in bold typeface and underlined, and deletions are in bold typeface and enclosed in brackets.

The paragraph starting on page 3, line 7 is amended as follows.

FIG. 2 is a partial perspective view that shows **[an enlargement of part]** **the structure of the semiconductor chip and the conductive bump** of the semiconductor package of FIG. 1.

The paragraph starting on page 3, line 15 is amended as follows.

Use of the same reference symbols **in different drawings** indicates similar or identical items.

The paragraph starting on page 3, line 22 is amended as follows.

FIG. 1 shows a semiconductor package 100 in accordance with an embodiment of the present invention. In the semiconductor package 100, a semiconductor chip 10, which has conductive bumps 16 on an active surface of **the** chip 10, is on a substrate 20, such that the conductive bumps 16 connect to bonding pads 22 formed on the substrate 20. The substrate 20 further includes external terminals 21 for electrically connecting the semiconductor chip 100 to an external component. The bonding pads 22 electrically connect to respective external terminals 21 through a circuit pattern (not shown) formed, for **[examlpe]** **example**, in the substrate 20. The external terminals 21 can have various forms, such as straight leads, gull-wing type leads, and solder balls. As an example, the external terminals 21 of FIG. 1 are straight leads.

The paragraph starting on page 4, line 3 is amended as follows.

Between the chip 10 and the substrate 20, an under-filling portion 50 is formed to prevent cracking of the conductive bumps 16 due to the thermal expansion mismatch between

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the chip 10 and the substrate 20. Then, in order to promote the heat dissipation from the chip 10, a plate-shaped heat slug 40 is attached on the backside of the chip 10, on which an adhesion layer 14 is formed, using a solder film 30. The heat slug 40 is formed of a metal such as Cu, Al or CuW. In addition, grooves 43 are formed on the heat slug 40 to facilitate the heat dissipation by increasing the surface area of the heat slug 40. In addition, an adhesion layer (not shown), which is typically a Ni/Al, Ag, or Pd layer, can be formed on one side 41 of heat slug 40 contacting the solder film 30 to secure the bonding between the heat slug 40 and the conductive solder film 30, and an anodizing layer (not shown) is formed on the other side of the heat slug 40 to prevent oxidation of the heat slug 40. The solder film 30 is formed of a metal alloy which includes Pb, Sn, Ag, In and/or Bi. Such metal alloy typically has thermal conductivity of 25W/mK to 40W/mK and good adhesion strength. The solder film 30 preferably has a size equal to or greater than that of the semiconductor chip 10, so that the solder film 30 covers the whole backside of the chip 20. The **adhesion** layer 14, which promotes the adhesion between the semiconductor chip 10 and the solder film 30, typically has a multi-layer metal structure. Exemplary structures of the layer 14 include VNi/Au, Ti/VNi/Au, Cr/VNi/Au, Ti/Pt/Au, Cr/CrCu/(Cu)/Au, TiW/(Cu, NiV)/Au, VNi/Pd, Ti/VNi/Pd, Cr/VNi/Pd, Ti/Pt/Pd, Cr/CrCu/(Cu)/Pd, and TiW/(Cu, NiV)/Pd.

The paragraph starting on page 5, line 30 is amended as follows.

In preparing the semiconductor chip 10 of FIG. 4A, the under-bump metallurgy (UBM) layer 17, which includes Cr, Cr/Cu, and Cu layers, is formed on the chip pads (not shown) of the semiconductor substrate 11, in and on which circuits (not shown) have been formed, by known sputtering and patterning. Typically, the semiconductor substrate 11 is a silicon wafer. On the patterned UBM layer 17, under which the chip pads are, the conductive bumps 16 are formed. Then, the **[metal]** **adhesion** layer 14 is formed on the backside of the semiconductor substrate 11 by sputtering, evaporation, electro-plating, or electroless-plating. As previously described, the metal layer 14 is formed of a multi-layer metal film such as VNi/Au, Ti/VNi/Au, Cr/VNi/Au, Ti/Pt/Au, Cr/CrCu/(Cu)/Au, TiW/(Cu, NiV)/Au, VNi/Pd, Ti/VNi/Pd, Cr/VNi/Pd, Ti/Pt/Pd, Cr/CrCu/(Cu)/Pd, or TiW/(Cu, NiV)/Pd.

The paragraph starting on page 6, line 11 is amended as follows.

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Before the forming of the **[metal]** **adhesion** layer 14, the backside of the semiconductor substrate 11 can be chemically cleaned using an HF solution to strengthen the bonding between the semiconductor substrate 11 and the **[metal]** **adhesion** layer 14. The cleaning process can be carried out by plasma cleaning.

The paragraph starting on page 6, line 16 is amended as follows.

The formation of the UBM layer 17 and the conductive bump 16, and the formation of the **[metal]** **adhesion** layer 14 can be performed in a reverse order. After the formation of UBM layer 17, the conductive bump 16, and **[metal]** **adhesion** layer 14, the semiconductor substrate in a wafer form is divided into multiple pieces of semiconductor chips 10 by sawing process.

The paragraph starting on page 6, line 21 is amended as follows.

[Regarding] **Referring** to FIG. 4B, in order to attach the heat slug 40 to the backside of the semiconductor chip 10, a bonding apparatus (not shown) aligns the heat slug 40 and the solder film 30 on the backside of the semiconductor chip 10, and applies heat to the aligned elements under H_2 environment. The heat application medium can be a furnace or a thermode pressing the heat slug 40 from the top.

The paragraph starting on page 6, line 27 is amended as follows.

[Regarding] **Referring** to FIG. 4C, the semiconductor chip 10 with the heat slug 40 attached thereon is attached to the substrate 20. The semiconductor chip 10 is placed on the substrate 20 with the conductive bumps 16 of the semiconductor chip 10 on respective bonding pads of the substrate 20. Then, heating in a reflow furnace attaches the semiconductor chip 10 to the substrate 20. Alternatively, an adhesive layer (not shown), which bonds the conductive bumps 17 to the respective bonding pads 22, attaches the semiconductor chip 10 to the substrate 20. After the bonding between the conductive bumps 17 and the respective bonding pads 22, liquid resin is injected into the space between the semiconductor chip 10 and the substrate 20 to form the under-filling portion 50. Accordingly, the semiconductor package 100 has been completed.

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ATTACHMENT B

This response amends claims 1, 3, 6, 10, 11, 14, 15, and 20 as follows.

1. (Amended) A semiconductor chip package comprising:

a substrate having a plurality of bonding pads;

a semiconductor chip having a plurality of conductive bumps on a front side thereof, the conductive bumps contacting the bonding pads;

a heat slug bonded to a backside of the semiconductor chip; and

a solder film that bonds the heat slug to the backside of the semiconductor chip.[.]

3. (Amended) The semiconductor chip package of claim 1 wherein the backside of the semiconductor chip includes a metal layer formed thereon for strengthening [the] adhesion between the semiconductor chip and the [metal] solder film.

6. (Amended) The semiconductor chip package of claim 1, wherein the solder film has a size equal to or [lager] larger than a size of the semiconductor chip.

10. (Amended) The semiconductor chip package of claim 1, wherein the heat slug is coated with an anodizing layer on a surface of the heat slug that is opposite to another surface of the heat slug, on which the semiconductor chip is bonded.

11. (Amended) The semiconductor chip package of claim 1, wherein the heat slug is shaped such that a portion of the heat slug is attached to the substrate by an adhesive.[.]

14. (Amended) A method of fabricating a semiconductor chip package, comprising:

preparing the semiconductor chip having a plurality of conductive bumps on a front surface of the semiconductor chip;

bonding a heat slug on a backside of the semiconductor chip using a solder film; and

attaching the semiconductor chip on a substrate such that the conductive bumps of the semiconductor chip contact[s] a plurality [o] of bonding pads on the substrate.

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15. (Amended) The method of claim 14, further comprising filling a resin into a space between the semiconductor chip and the substrate.

20. (Amended) The semiconductor chip package of claim 16, wherein the heat slug is coated with an anodizing layer on a surface of the heat slug that is opposite to another surface of the heat slug, on which the semiconductor chip is bonded.

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ATTACHMENT C

In the following, insertions are in bold typeface and underlined, and deletions are in bold typeface and enclosed in brackets.

The paragraph starting on page 12, line 3 is amended as follows.

The present invention is directed to a semiconductor chip package that can effectively remove heat from a semiconductor chip, and a method of fabricating the package. In accordance with an embodiment of the invention, the package includes: a substrate having bonding pads; a semiconductor chip having conductive bumps on the front side thereof, the conductive bumps contacting the bonding pads; a heat slug bonded to the backside of the semiconductor chip; and a solder film which makes the bonding between the heat slug and the backside of the semiconductor chip. The heat slug can be shaped such that a portion of the heat slug is attached to the substrate by an adhesive. The method includes: preparing a semiconductor chip having conductive bumps on the front surface of the semiconductor chip; bonding a heat slug on the backside of the semiconductor chip using a solder film; and attaching the semiconductor chip on the substrate such that the conductive bumps of the semiconductor chip contact**[s]** bonding pads of the substrate.

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